Department of Information Science & Engineering

Course: Digital Design Lab [P18ISL38]

SEM: III

Staff: BRAMESH S M

Lab Manual & Syllabus: https://sites.google.com/view/brameshsm/2020-21-odd-sem

Lab site introduction: https://youtu.be/hlqorYI76cY

Link to download tool: https://drive.google.com/drive/folders/1c6tfbny8vxN-we8-FaB2NzTAelKRQcs3?usp=sharing

Sl. No.	Experiment Title	Link
1	Logic Gates	https://youtu.be/5a1niMEWNNc https://youtu.be/w2uy4OM6DTU
2.	Design a circuit for Full Adder Using Logic Gates	https://youtu.be/Zxq_ZRMjcEc
3.	Application of Decoder.	https://youtu.be/5gPDpGbGpPQ
4.	Design of Ring Counter/Johnson Counter.	https://youtu.be/sfAqGVTR7rk
5.	Application of MUX/DEMUX.	https://youtu.be/cqoTrRJDhNE
6.	Tool introduction with Basic Gates simulation	https://youtu.be/wE1lqB8kz2s
7.	Simulating Full Adder	https://youtu.be/MSGfJsEjZtc
8.	Simulating 8:1 MUX	https://youtu.be/LDPOjAvsCX8
9.	Simulating D-FF	https://youtu.be/5BiN4nQrzrg
10.	Simulating MOD-8 Up Counter	https://youtu.be/QB5ZKGCwVuc
11.	Simulating Ring and Johnson counter	https://youtu.be/JJtoHOuHnTY