Scheme & Syllabus
Of

M.Tech in VLSI Design and Embedded Systems
Department of Electronics and Communication Engineering
(With effect from 2020-2021 Academic year)

Outcome Based Education
with
Choice Based Credit System

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(±ÉÊPÀëtÂPÀªÀµÀð 2020-21)

P.E.S. College of Engineering, Mandya - 571 401, Karnataka
(An Autonomous Institution Affiliated to VTU, Belagavi,
Grant -in- Aid Institution (Government of Karnataka), World Bank Funded College (TEQIP)
Accredited by NBA & NAAC and Approved by AICTE, New Delhi.)

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P.E.S COLLEGE OF ENGINEERING, MANDYA-571401
(KARNATAKA)
(An Autonomous Institution under VTU, Belagavi)

Vision

PESCE shall be a leading Institution imparting quality Engineering and Management Education developing creative and socially responsible professionals.

Mission

- Provide state of the art infrastructure, motivate the faculty to be proficient in their field of Specialization and adopt best teaching-learning practices.
- Impart engineering and managerial skills through competent and committed faculty using Outcome based educational curriculum.
- Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the Societal needs.
- Promote research, product development and industry-institution interaction.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

About the Department:

The department of Electronics and Communication Engineering was incepted in the year 1967 with an undergraduate program in Electronics and Communication Engineering. Initially program had an intake of 60 students and presently 150 students graduate every year. The long journey of 50 years has seen satisfactory contributions to the society, nation and world. The alumni of this department have strong global presence making their alma mater proud in every sector they represent.

Department has started its PG program in the year 2012 in the specialization of VLSI design and Embedded systems. Equipped with qualified and dedicated faculty department has focus on VLSI design, Embedded systems and Image processing. The quality of teaching and training has yielded high growth rate of placement at various organizations. Large number of candidates pursuing research programs (M.Sc/Ph D) is a true testimonial to the research potential of the department.

Vision

The department of E & C would endeavour to create a pool of Engineers who would be **extremely competent technically, ethically strong** also fulfil their obligation in terms of **social responsibility**.

Mission

- **M1:** Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience conducive to imbibe technical knowledge and practicing ethics.
- **M2**:Group and individual exercises to inculcate habit of analytical and strategic thinking to help the students to develop creative thinking and instil team skills
- **M3**:MoUs and Sponsored projects with industry and R & D organizations for collaborative learning
- **M4**:Enabling and encouraging students for continuing education and moulding them for life-long learning process.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(A) Programme Learning Objectives (PLOs)

M.Tech in VLSI Design and Embedded system during two years term, aims to

1. Provide the students with strong fundamental and advanced knowledge in VLSI Design and Embedded system with an emphasis to solve engineering problems.
2. Train the students in VLSI and Embedded system design tools and make them fit for the industries.
3. Inculcate in students the professional and ethical attitude, effective communication skills, team spirit and nurture them as leaders.
4. Provide teaching skills and inculcate spirit of research.
5. Motivate to continue education leading to doctoral degree and choose research as career option.

(B) Programme Outcomes (POs):

The Master of Technology Programme in Electronics and Communication Engineering [M.Tech in VLSI Design and Embedded systems] must demonstrate that it's Post graduates have

1. An ability to apply knowledge gained out of this program to develop products and solutions in the area of VLSI design and Embedded Systems.
2. An understanding of professional and ethical responsibilities at national and international levels.
3. An ability to effectively communicate both written and oral on social and technical problems at national and global scenarios.
4. An ability to engage in independent and lifelong learning in the broad context of technological change.
5. Ability to carry- out independent research.

A total of 88 credits for 2 years M.Tech programme

Credit pattern

Core Courses: - I Semester 12 credits
II Semester 12 credits
Total credits for core courses is 24 credits
Elective Course: - I Semester 08 credits
II Semester 08 credits
Total credits for Elective courses is 16 credits
Self Study course: - 06 credits
Seminar: - 02 credits
Lab: - 04 credits
Industrial Training: - 06 credits
Research Methodology: - 04 credits
Mini Project: 02 credits
Term Paper:- 02 credits
Project work:- 22 credits. A total of 88 credits for 2 years M.Tech programme

Category of Courses:

1. Core Courses: The Core courses constitute the core of the programme of study. Core courses are to be compulsorily studied by a student and are mandatory to complete them to fulfill the requirements of a programme.

2. Professional Electives: Elective courses offer a choice of advanced or specialized courses related to the programme of study. They enable students to specialize in a domain of interest or tune their learning to suit career needs and current trends.

3. Laboratories: The Laboratories are evaluated for 100 marks which includes CIE: 50 marks & SEE: 50 marks. The assessment of CIE is done with execution of lab programs & report submission. The final SEE assessment is done with the conduction of exam and Viva-Voce.

4. Self-Study Course: The Self-Study Course should be chosen from the available 12 weeks NPTEL online courses recommended by the Department. The student can undergo NPTEL course registration during II / III Semester and the credit will be considered in III Semester. The 100 marks CIE assessment is based on the final NPTEL score (i.e. Online assignments: 25% + Proctored exam: 75%). The NPTEL score will be mapped directly to the CIE marks only if he /she has completed the NPTEL course (i.e. Certification). Those, who do not take-up/ Complete the NPTEL course shall be declared as failed and have to complete during the subsequent examination after satisfying the NPTEL requirements.

5. Internship: All the students have to undergo mandatory internship of 8 weeks during the vacation of I and II semesters and / or II and III semesters. An examination shall be conducted during III semester and the prescribed credit shall be counted for the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/ Complete the internship shall be declared as failed and have to complete during the subsequent examination after satisfying the internship requirements.

6. Technical Seminar: CIE marks shall be awarded by a committee comprising of HOD as Chairman, Guide/co-guide, in any and a senior faculty of the department. Participation in seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory. The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

7. Mini Project:

- Mini Project shall comprise of an exercise assigned to a student similar to major projects.
- The topics may be related to the field of their UG Programme, that address the social issues.
- A report (not less than 20 A4 pages) to be submitted, detailing the solution to the problem / concept worked out during the semester.

- The work may be evaluated for award of Internal Assessment marks (CIE) based on a presentation / demonstration and viva voce, by a committee coordinated by the Course coordinators.

8. Project Work: The Project Work carries 22 credits and spreads over THREE semesters, i.e. during II, III and IV semesters. Project work Phase-1, 2 & 3 to be awarded by the Department committee constituted for the purpose.

- The **Project Phase-I** evaluation shall be of 100 marks CIE. It is based on the submission report consisting of Title, Introduction, Literature Survey, Objectives and Methodology (50 Marks) and Presentation (50 marks).
- The **Project Phase-II** evaluation shall be of 100 marks CIE. It is based on submission report consisting of theoretical analysis and design approach of the work (50 Marks) and Presentation for 50 marks.
- The **Project Phase-III** evaluation shall be of 100 marks CIE. It is based on the overall completion &demonstration / execution of the project (50 Marks) and presentation for 50 marks.
- The **Project Phase Thesis** evaluation shall be of 100 marks each for CIE& SEE. The Thesis Evaluation done by Internal Examiner & External examiner shall be considered for CIE & SEE marks respectively.
- The **Project Phase Viva Voce** evaluation shall be of 100 marks SEE. It is based on Thesis presentation and project viva voce has to be conducted jointly by internal and external examiner for a total of 100 marks SEE.

9. Term Paper: The term paper is purely based on the project work he/she chooses.

- The Term paper shall be for 100 marks CIE only. It has to be evaluated by the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate.
- The term paper evaluation is based on the publication of an article in peer reviewed conference/ journal (national/ international) and quality of the journal. If the term paper is not published by the candidate or the same is communicated for publication at the end of his/ her tenure, then the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate will assess for the award of credit.

SCHEME OF TEACHING AND EXAMINATION

I SEMESTER M.TECH IN VLSI DESIGN AND EMBEDDED SYSTEMS

Sl. No.	Course Code	Course Title	Teaching Department	Hrs / Week	Credits	Examination Marks		
				L:T:P:H		CIE	SEE	Total
1	P20MECE11	CMOS VLSI Design	ECE	4:0:0:4	4	50	50	100
2	P20MECE12	Embedded System Design	ECE	4:0:0:4	4	50	50	100
3	P20MECE13	Physical Design	ECE	4:0:0:4	4	50	50	100
4	P20MECE14X	Professional Elective – I	ECE	4:0:0:4	4	50	50	100
5	P20MECE15X	Professional Elective – II	ECE	4:0:0:4	4	50	50	100
6	P20MECEL16	Laboratory –I	ECE	0:0:4:4	2	50	50	100
7	P20MECE17	Mini Project	ECE	--	2	50	50	100
Total					**24**	**350**	**350**	**700**

Professional Elective – I			**Professional Elective – II**		
Sl. No.	**Course Code**	**Course Title**	**Sl. No.**	**Course Code**	**Course Title**
1	P20MECE141	Advances in IC Fabrication Technology	1	P20MECE151	ASIC Design
2	P20MECE142	Digital System Design using Verilog	2	P20MECE152	Multicore Architecture and Programming
3	P20MECE143	System on Chip	3	P20MECE153	MEMS and Sensors

SCHEME OF TEACHING AND EXAMINATION

II SEMESTER M.TECH IN VLSI DESIGN AND EMBEDDED SYSTEMS

Sl. No.	Course Code	Course Title	Teaching Department	Hrs / Week	Credits	Examination Marks		
				L:T:P:H		CIE	SEE	Total
1	P20MECE21	CMOS Mixed Mode VLSI Circuits	ECE	4:0:0:4	4	50	50	100
2	P20MECE22	Low Power VLSI Design	ECE	4:0:0:4	4	50	50	100
3	P20MECE23	Automotive Electronics Design Fundamentals	ECE	4:0:0:4	4	50	50	100
4	P20MECE24X	Professional Elective – III	ECE	4:0:0:4	4	50	50	100
5	P20MECE25X	Professional Elective – IV	ECE	4:0:0:4	4	50	50	100
6	P20MECE26	Project Phase-I	ECE	0:0:0:0	2	100	-	100
7	P20MECEL27	Laboratory –II		0:0:4:4	2	50	50	100
Total					**24**	**400**	**300**	**700**

Professional Elective – III			**Professional Elective – IV**		
Sl. No.	**Course Code**	**Course Title**	**Sl. No.**	**Course Code**	**Course Title**
1	P20MECE241	ARM Processors	1	P20MECE251	System Verilog for Design and Verification
2	P20MECE242	Embedded System Design with FPGA	2	P20MECE252	Design of VLSI Systems
3	P20MECE243	Robotics and Automation	3	P20MECE253	RF Integrated Circuits

Course Title: **CMOS VLSI Design**			
Course Code: **P20MECE11**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the basic knowledge of MOSFETs.
2. Discuss the MOS Transistor threshold voltage equation.
3. Describe the second order effects.
4. Provides the knowledge of lambda based design rule and process technology
5. Outline the concepts of Basics of Digital CMOS Design.
6. Discuss the concepts of clocking in digital CMOS design
7. Describe the different types of semiconductor memories.

B. Course Content

UNIT – I

MOS Transistor Theory : Introduction, Long-Channel I-V Characteristics, C-V Characteristics, Nonideal I-V Effects, Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Leakage, Temperature Dependence, Geometry Dependence, DC Transfer Characteristics, Static CMOS Inverter DC Characteristics, Beta Ratio Effects, Noise Margin, Pass Transistor DC Characteristics.

CMOS Processing Technology : Introduction, CMOS Technologies, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Isolation, Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, Metrology, Layout Design Rules, Design Rule Background, Scribe Line and Other Structures, MOSIS Scalable CMOS Design Rules, Micron Design Rules

Text 1: Chapter 2, 3 **11 Hrs**

Self Learning Components:

1. Introduction to Cadence environment Tool, create schematic and symbol, introduction to netlist, technology library.
2. DC and transient analysis of CMOS inverter.

UNIT – II

CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS, Technology-Related CAD Issues: Design Rule Checking (DRC), Circuit Extraction, Manufacturing Issues: Antenna Rules, Layer Density Rules, Resolution Enhancement Rules, Metal Slotting Rules, Yield Enhancement Guidelines

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Effort of Paths, Timing Analysis Delay Models.

Power: Introduction, Dynamic Power, Static Power, Energy-Delay Optimization, Low Power Architectures

Text 1: Chapter 3, 4, 5 **10 Hrs**

Self Learning Components:

1. Layout, DRC, LVS, Extract RC and back annotate the same and verify the Design of CMOS Inverter.

UNIT – III

Circuit Simulation: Introduction, A SPICE Tutorial, Device Models, Device Characterization, Circuit Characterization, Interconnect Simulation.

Combinational Circuit Design: Introduction, Circuit Families, Circuit Pitfalls, More Circuit Families, Silicon-On-Insulator Circuit Design, Subthreshold Circuit Design.

Text 1: Chapter 8, 9 **10 Hrs**

Self Learning Components:

1. Design and Analysis of NAND, NOR and complex gates

UNIT – IV

Sequential Circuit Design: Introduction, Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining.

Dynamic Logic Circuits: Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping.

Text 1: Chapter 10 **11 Hrs**

Text 2: Chapter 9

Self Learning Components:

1. Design and characterization of Transmission gates, Latches and Flip-flops

UNIT – V

Chip Input And Output (O) Circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution , Latch-Up and Its Prevention

Semiconductor Memories: Introduction, Read-Only Memory (ROM) Circuits, Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuit.

Text 2: Chapter 10, 13 **10 Hrs**

Self Learning Components:

1. Case study: Study on Different Integrated circuits. (https://www.youtube.com/watch?v=QXBlQZYGO6Y)
2. CMOS VLSI Applications (https://ieeexplore.ieee.org/document/1146652)

TEXT BOOKS:

1. ***"CMOS VLSI Design: a Circuits and Systems Perspective",*** Neil H. E. Weste, David Money Harris, Pearson, 4th edition, ISBN 10: 0-321-54774-8, ISBN 13: 978-0-321-54774-3
2. **"CMOS Digital Integrated Circuits: Analysis and Design**", Sung Mo Kang & Yosuf Lederabic Law, McGraw-Hill, 3rd edition , ISBN: 9780071243421, 9780071243421.

REFERENCE BOOKS:

1. **"Digital Integrated Circuits: A Design Perspective"**, Jan M. Rabey, Anantha Chadrakasan, 2nd edition, Pearson, ISBN-13: 978-0130909961, 2016
2. "**Modern VLSI design: System on Silicon" Pearson Education**", Wayne, Wolf, 2nd edition, ISBN: 81-7758-411-1, 1998.
3. "**Basic VLSI Design**" Douglas A Pucknell & Kamran Eshragian , PHI 3rd edition (original Edition – 1994), ISBN:978-81-203-0986-9.
4. **"Introduction to VLSI Circuits and systems"**, John .P. Uyemura, John Wiley.
5. **"CMOS DIGITAL VLSI DESIGN"**, by PROF. SUDEB DASGUPTA (IIT Roorkee) https://nptel.ac.in/courses/108/107/108107129/ .

Course Title: **Embedded Systems Design**			
Course Code: **P20MECE12**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%** SEE: **50%**	

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide general approach to Embedded System (ES) design
2. Make one to understand use of ARM and PIC microcontrollers in ES design
3. Understand the role of different CPU components in ES design and their influence on performance
4. Provide understanding of different performance analysis
5. Provide understanding of different programming models
6. Provide knowledge of OS fundamentals and approach to scheduling algorithms
7. Provide understanding of program optimization, safety and security design issues
8. Discuss different issues of inter process communication

B. Course Content

UNIT – I

Introduction: Introduction, Complex Systems and Microprocessors, The embedded system design process, Programmer Interface to the hardware – Preliminaries, ARM Processor and PIC micromirrange family

Text 1: Chapter 1 and 2 **11 Hrs**

Self Learning Components:

Design Example: model Train Controller 2. Differentiate programming ARM and PICmicro taking FIR filter example

UNIT – II

CPU Components: Programming Input and Output, Interrupts (only ARM and PIC to be considered) , Supervisor mode, exceptions and traps, Coprocessors, Memory System mechanisms, CPU Performance, Safety and security

Basic Computing Platforms, The CPU BUS, Memory Devices and Systems

Text 1: **Chapter 3 and 4** **10 Hrs**

Self Learning Components:

Design Example: Data Compressor

UNIT – III

Designing of Embedded Systems: Platform Dependency, Architecture for Consumer Electronics systems, Platform level performance analysis and power management

Components of Embedded programs, models for programs, Program-level performance analysis, software performance optimization, program validation and testing, safety and security

Text 1: **Chapter 4 and 5** **11 Hrs**

Self Learning Components:

Design Example: Audio player and Digital still camera

UNIT – IV

Real-Time Operating System (RTOS): Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS (Only conceptual understanding, no programming implementation).

Text 2: Chapter 10 **10 Hrs**

Self Learning Components:

Implementation of scheduling schemes

UNIT – V

System Design Techniques and Embedded Multiprocessors: System Design Techniques: Design Methodologies, Requirement Analysis, Specifications, System analysis and architecture design, dependability, safety and security

Embedded Microprocessors: Introduction, Why multiprocessors? Categories of multiprocessors, MPSOCs and shared memory multiprocessors, Application Example – Optical Disk

Text 1: **Chapter 7and 10** **10 Hrs**

Self Learning Components:

Design example: Video Accelerator

TEXT BOOKS:

1. **"Computers as Components- Principles of Embedded Computing System Design",** by Marilyn Wolf , 4th edition, Morgan Kaufman Publications, ISBN: 978-0-12-805387-4, 2017.
2. **"Introduction to Embedded Systems",** Shibu K V, TMH Education Pvt Ltd, 2nd reprint, ISBN (13): 978-0-07-014589-4, 2010.

REFERENCE BOOKS:

1. **"Embedded Systems – A contemporary Design Tool"**, James K Peckol, John Weily, Edition, ISBN-13: 978-0471721802, ISBN-10: 9780471721802, 2008.
2. **"Embedded Systems Design: An Introduction to Processes, Tools, and Techniques"** Arnold S. Berger, ISBN: 1578200733 CM.

Course Title: **Physical Design**			
Course Code: **P20MECE13**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing.
2. Describe the concept behind the VLSI design rules and routing techniques
3. Discuss the concepts of design optimization algorithms and their application to physical design automation.
4. Understand the concepts of simulation and synthesis in VLSI Design Automation

B. Course Content

UNIT – I

Introduction to Electronic Design Automation, VLSI Design Flow, VLSI Design Styles, Layout Layers and Design Rules, Physical Design Optimizations, Algorithms and Complexity, Graph Theory Terminology.

Netlist and System Partitioning: Introduction, Terminology, Optimization Goals, Partitioning Algorithms: Kernighan-Lin (KL) Algorithm.

Text 1: Chapter 1 and 2 **10 Hrs**

Self Learning Components:

Learn Tool Command Language (TCL).

UNIT – II

Chip Planning: Introduction, Optimization goals in Floor planning, Terminology, Floor plan representations, **Floor Planning Algorithms:** Floor plan sizing, cluster growth, simulated annealing, Pin assignment, **Power and Ground Routing:** Design of Power-Ground Distribution Network, Planar Routing, Mesh Routing.

Text 1: Chapter 3 **10 Hrs**

Self Learning Components:

Analyse the synthesis report files for Area, Power and Timing

UNIT – III

Global Placement and Routing: Introduction, Optimization Objectives, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, Modern placement algorithms.

Global Routing: Introduction, Terminology and Definitions, Optimization Goals, Routing terminology and goals, Representations of Routing Regions, The Global Routing Flow, Single-Net Routing**:** Rectilinear routing, Finding Shortest Paths with Dijkstra's Algorithm, , Full net routing: Routing by Integer Linear Programming, Rip-up and Re-route, Modern Global Routing.

Text 1: Chapter 4 and 5 **11 Hrs**

Self Learning Components:

For a design generate the area report through synthesis and calculate the Floorplan size for a design

UNIT – IV

Clock Routing , Clocking Schemes, Design Considerations for the Clocking System, Problem Formulation, Clock Routing Algorithms, Skew and Delay Reduction by Pin Assignment, Multiple Clock Routing.

Design for manufacturability and reliability in extreme-scaling VLSI

Text 2: Chapter 11.

Text 3: Paper **10 Hrs**

Self Learning Components:

Demonstration the place and route steps for any design using cadence innovous/encounter

UNIT – V

Timing Closure: Introduction, Timing Analysis and Performance Constraints, Timing-Driven Placement, Timing-Driven Routing, Physical Synthesis, Performance-Driven Design Flow.

Text1: Chapter 8 **11 Hrs**

Self Learning Components:

Demonstration the clock tree synthesis steps for any design using cadence innovous/encounter

TEXT BOOKS:

1. **"VLSI Physical Design: From Graph Partitioning to Timing Closure"**, Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, 1st edition, Springer, 2011 ISBN 978-90-481-9590-9 e-ISBN 978-90-481-9591-6
2. "**Algorithms for VLSI Physical Design Automation"**, N. A. Shervani, 1999. 3rd edition ISBN 0-7923-8393-1
3. "**Design for Manufacturability and Reliability in Extreme-Scaling VLSI**," B. Yu, X. Xu, S. Roy, Y. Lin, J. Ou, and D. Z. Pan, Science China Information Sciences, pp. 1--23, 2016. https://www.cerc.utexas.edu/utda/publications/J63.pdf

REFERENCE BOOKS:

1. **"Algorithms for VLSI Design Automation"**, Sabih H. Gerez, ISBN: 9780471984894, 0471984892, 2000.
2. **"Handbook of Algorithms for Physical design Automation",** Charles J. alpert, Dinesh p. Mehta, Sachin S. Sapatnekar. ISBN: 9780849372421, 0849372429
3. "**Digital VLSI Design (RTL to GDS)**" Dr. Adam Teman , Emerging nanoscaled Integrated Circuits and Systems (EnICS) Labs Faculty of Engineering, Bar-Ilan University https://www.youtube.com/watch?v=RbZ3BXbd6_k&list=PLZU5hLL_713x0_AV_rVbay0pWmED7992G
4. https://www.vlsisystemdesign.com/Clock-Tree-Synthesis-Video-Series.php

Professional Elective-I			
Course Title: **Advances in IC Fabrication Technology**			
Course Code: **P20MECE141**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%** SEE: **50%**	

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the overview of crystal growth technique and thin film technologies.
2. Explain the different lithographic process, plasma formation and etching techniques,
3. Describe the deposition process of polysilicon, oxide, nitride and other materials.
4. Highlight the ion implantation techniques with shallow and deep profiles.
5. Discuss the metallization process and VLSI NMOS and PMOS fabrication processes.
6. Provide the steps of IC memory fabrication technology and packaging schemes.

B. Course Content

UNIT – I

Crystal Growth and Doping: Starting Growth and Doping, Growth from the Melt, Considerations for Proper Crystal Growth, Doping in the Melt, Semi-Insulating Gallium Arsenide, Properties of Melt-Grown Crystals, Solution Growth, Zone Processes, Properties of Zone-Processed Crystals.

Text 1: Chapter 3 **11 Hrs**

Self Learning Components:

Case study on 45 nm CMOS node Process technology

UNIT – II

Diffusion: The Nature of Diffusion, Diffusion in a Concentration Gradient, The Diffusion Equation, Impurity Behavior: Silicon, Impurity Behavior: Gallium Arsenide, Diffusion Systems, Diffusion Systems for Silicon, Special Problems in Silicon Diffusion, Diffusion Systems for Gallium Arsenide, Evaluation Techniques for Diffused Layers.

Text 1: Chapter 4 **10 Hrs**

Self Learning Components: Case study on evaluation techniques in diffusion.

UNIT – III

Epitaxy: General Considerations, Molecular Beam Epitaxy, Vapor-Phase Epitaxy, VPE Processes for Silicon, VPE Processes for Gallium Arsenide, Liquid-Phase Epitaxy, LPE Systems, Heteroepitaxy, Evaluation of Epitaxial Layers.

Text 1: Chapter 5 **11 Hrs**

Self Learning Components:

New trends in the Epitaxy methods.

UNIT – IV

Ion Implantation: Penetration Range, Implantation Damage, Annealing, Ion Implantation Systems, Process Considerations, High-Energy Implants, High-Current Implants.

Etching and Cleaning: Wet Chemical Etching, Dry Physical Etching, Dry Chemical Etching, Reactive Ion Etching.

Text 1: Chapter 6 and 9 **10 Hrs**

Self Learning Components:

Study on SOI devices and their applications.

UNIT – V

Lithographic Processes: Photo reactive Materials, Pattern Generation and Mask-Making, Pattern Transfer.

Device and Circuit Fabrication: Isolation, Self-Alignment, Local Oxidation, Planarization, Metallization, Gettering.

Text 1: Chapter 10 and 11 **10 Hrs**

Self Learning Components:

Study on Fully depleted Silicon on Insulator (FDSOI) devices and their applications.

TEXT BOOK:

1. **"VLSI Fabrication Principles: Silicon and Gallium Arsenide",** Gandhi, S. K., John Wiley and Sons, 2nd edition, ISBN: 978-0-471-58005-8, 2008.

REFERENCE BOOKS:

1. **"Silicon VLSI Technology: Fundamentals, Practice and Modeling",** Plummer J.D., Deal, M.D. and Griffin, P.B., Pearson Education, 3rd edition, Prentice-Hall, ISBN 978-81-317-2604-4, 2000.
2. **"VLSI Technology",** S.M.Sze , 2nd edition, McGraw-Hill, ISBN13: 9780070627352 ISBN10: 0070627355, 2003.
3. **"ULSI Technology",** C. Y. Chang & S. M. Sze (Editors), McGraw Hill, ISBN-10: 0070630623, ISBN-13: 978-0070630628, 1996.

VIDEO LECTURE:

1. https://nptel.ac.in/courses/117/106/117106093/#watch Lectured by Prof.Nandita Dasgupta, IIT Madras.

Professional Elective-I			
Course Title: **Digital System Design using Verilog**			
Course Code: **P20MECE142**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%** SEE: **50%**	

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand the concepts of Real world circuits, Models and Design methodology
2. Design and develop the Combinational and Sequential Circuits and verify using HDL.
3. Develop the Verilog coding for many applications.
4. Analyze the synthesis of Combinational and Sequential Logic.
5. Design and synthesis the datapath controllers.

B. Course Content

UNIT – I

Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.
Combinational Basics: Boolean Functions and Boolean algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits. **11 Hrs**
Text 1: Chapter 1 and 2
Self Learning Components:
Design and verify the combination circuits for the given specification using Boolean functions.

UNIT – II

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.
Sequential Basics: Storage elements, Counters, Sequential Datapath and Control, Clocked Synchronous Timing Methodology. **11 Hrs**
Text 1: Chapter 3 and 4
Self Learning Components:
Design and develop the Verilog model for the Synchronous and Asynchronous sequential circuits for the given specification.

UNIT – III

Memories: Concepts, Memory Types, Error Detection and Correction.
Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **10 Hrs**
Text 1: Chapter 5 and 6
Self Learning Components:
Design and verify the SRAM and DRAM for given specifications.

UNIT – IV

Synthesis of Combinational and Sequential Logic: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-State Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit

State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers, and Counters, Resets, Synthesis of Gated Clocks and Clock Enables. **10 Hrs**

Text 2: Chapter 6.1 to 6.11

Self Learning Components:

Synthesize the digital circuits using EDA tools.

UNIT – V

Design and Synthesis of Datapath Controllers: Partitioned Sequential Machines, Design Example: Binary Counter, Design and Synthesis of a RISC Stored-Program Machine, Design Example: UART.

Text 2: Chapter 7 **10 Hrs**

Self Learning Components:

Case Study for designing Datapath controllers

TEXT BOOKS:

1. "**Digital Design: An Embedded Systems Approach Using VERILOG",** Peter J. Ashenden, Elesvier, ISBN 978-0-12-369527-7(2008), 9788131216637(2009), 2010.
2. "A**dvanced Digital Design With the Verilog HDL"**, Michael D. Ciletti, 2nd edition, PHI, ISBN: 978–0–07–338054–4 2015.

REFERENCE BOOK:

1. "**Verilog HDL: A Guide to Digital Design and Synthesis**" Samir Palnitkar 2nd edition Pearson, ISBN: 9788177589184 (2003) 2013.

VIDEO LECTURE:

1. https://nptel.ac.in/courses/106/105/106105165/#download_videos Lectured by Prof. Indranil Sengupta, IIT Kharagpur.

Professional Elective-I			
Course Title: **System on Chip**			
Course Code: **P20MECE143**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Compare the performance, advantages, and disadvantages of system on board, system on chip, and system in package.
2. Provide the overview of embedded processors with different architectures and embedded memories with scratchpad and cache concepts.
3. Describe the AMBA, NOC , Customization and Configurability

B. Course Content

UNIT – I

Evaluation of silicon process Technology, The Evolution of Design Methodology, What Is SOC Design?, SOC and Productivity. Comparison between System-on-Board, System-on-Chip, and System-in-Package. Motivation for SOC Design Review of Moore's law.

Introduction to the systems approach: system architecture: an overview, components of the System: processors, memories, and interconnects hardware and software: programmability, versus performance, processor architectures, processor: a functional view, processor: an architectural view, memory and addressing, soc memory examples, addressing: the architecture of memory, memory for soc operating system, system - level interconnection, bus - based approach, network - on - chip approach, an approach for soc design, requirements and specifications, design iteration, system architecture and complexity, product economics and implications for soc, dealing with design complexity.

Text 1: Chapter 1 **11 Hrs**

Self Learning Components:

1. Identify the applications of SOC in today electronics industry.
2. Prepare the report on the tools available for the SOC Design.

UNIT – II

Chip Basics: Time, Area, Power, Reliability, and Configurability. introduction, design trade – offs, five big issues in system - on - chip (soc) design, cycle time, the pipelined processor, defining a cycle, optimum pipeline, performance, die area and cost, processor area, ideal and practical scaling, power, area – time – power trade - offs in processor design, workstation processor, embedded processor, reliability, dealing with physical faults, error detection and correction

Processors: processor selection for soc: overview, examples: processor core selection, basic concepts in processor architecture, instruction set, some instruction set conventions, branches, interrupts and exceptions, basic concepts in processor microarchitecture, basic elements in instruction handling, the instruction decoder and interlocks, buffers: minimizing pipeline delays, more robust processors: vector, very long instruction word (VLIW), and superscalar, vector processors and vector instruction extensions, vector functional units, VLIW processors, superscalar processors, processor evolution and two examples, processor evolution and two examples.

Text 1:2.1-2.7, 3.2-3-12 **11 Hrs**

Self Learning Components:

1. Discuss the Area Estimate of Reconfigurable Devices.
2. Prepare the report on the recent Processor are used in Computers, laptop, mobiles

UNIT – III

Memory Design: system - on – chip and board - based systems, introduction, soc external memory: flash, soc internal memory: placement, the size of memory, scratchpads and cache memory, basic notions, cache organization, cache data, write policies, strategies for line replacement at miss time, fetching a line, line replacement, cache environment: effects of system, transactions, and multiprogramming, other types of cache, split i - and d - caches and the effect of code density, multilevel caches, limits on cache array size, evaluating multilevel caches, logical inclusion, virtual - to - real translation, soc (on - die) memory systems, board - based (off - die) memory systems, simple dram and the memory array, SDRAM and DDR SDRAM, memory buffers, models of simple processor – memory interaction, models of multiple simple processors and memory.

Text 1:4.1-4.16 **10 Hrs**

Self Learning Components:

1. Compare the difference between SDRAM and DDR SDRAM.
2. Prepare the report on in today electronics industry.

UNIT – IV

Interconnect: Introduction, overview: interconnect architectures, what is an NOC ?, bus: basic architecture, arbitration and protocols, bus bridge, physical bus structure, bus varieties, soc standard buses, AMBA, core connect, bus interface units: bus sockets and bus wrappers, analytic bus models, contention and shared bus, simple bus model: without resubmission, bus model with request resubmission, using the bus model: computing the offered occupancy, effect of bus transactions and contention time, beyond the bus: NOC with switch interconnects, soc interconnect switches, static networks, dynamic networks, some NOC switch examples, asynchronous crossbar interconnect for synchronous SOC, (dynamic network), blocking versus nonblocking, layered architecture and network, interface unit, NOC layered architecture, bus versus NOC, evaluating interconnect networks, static versus dynamic networks.

Text 1:5.1-5.9 **10 Hrs**

Self Learning Components:

1. Indentify the usage of AMBA in real time.
2. Discuss the tools are available for the NOC design.

UNIT – V

Customization and Configurability: introduction, estimating effectiveness of customization, soc customization: an overview, customizing instruction processors, processor customization approaches, architecture description, identifying custom instructions automatically, reconfigurable technologies, reconfigurable functional units (FUs), reconfigurable interconnects, software configurable processors , mapping designs onto reconfigurable devices, instance - specific design, reconfiguration, reconfiguration overhead analysis, trade - off analysis: reconfigurable parallelism,

Application Studies: AES - algorithm and requirements, - 3D graphics processors, image compression, video compression, MP3 audio decoding

Text 1:6.1-.6.9, 7.3-7.6 **10 Hrs**

Self Learning Components:

1. Compare the difference between AES and DES.
2. Identify the different algorithms used in video compression.

TEXT BOOK:

1. **"Computer System Design System-On-Chip"** Michael J. Flynn, Wayne Luk, A John Wiley & Sons, Inc., Publication, ISBN: 9781118009925, 2011.

REFERENCE BOOKS:

1. **"Reuse Methodology Manual for System-On-A-Chip",** Michael Keating, Designs, Pierre Bricaud, 2nd edition, Kluwer Academic Publishers, ISBN: 9781461550372, 2001.
2. **"SoC Verification-Methodology and Techniques",** Prakash Rashinkar, Peter Paterson and Leena Singh, Kluwer Academic Publishers, ISBN – 8580000264227, 2001.
3. **"On-Chip Communication Architectures: System on Chip Interconnect",** Sudeep Pasricha and BNikil B Dutt, Morgan Kaufmann Publishers, 978-0-12-373892-9, 2008.

Professional Elective-II			
Course Title: **ASIC Design**			
Course Code: **P20MECE151**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the knowledge of ASIC Design Flow.
2. Cover Fundamentals of Full custom, Semi custom and standard cell based design.
3. Provide the knowledge of low-level design entry.
4. Application of Low Level Design Languages.
5. Describe the various concepts of floor planning and placement and routing and partitioning methods.

B. Course Content

UNIT – I

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA, Design flow, ASIC cell libraries.

Text 1: 1.1- 1.3, 1.5 **10 Hrs**

Self Learning Components:

1. Understand the Comparison between ASIC Technologies.
2. Understand the concept of Product Cost, ASIC Fixed Costs.

UNIT – II

Data Path Logic Cells, Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers, ASIC Library Design: Logical effort, predicting delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum number of stages, library cell design.

Text 1: 2.6, 2.7, 3.3, 3.4 **11 Hrs**

Self Learning Components:

1. Discuss the CMOS Design Rules.
2. Discuss the Transistor Parasitic Capacitance- Junction Capacitance, Overlap Capacitance, Gate Capacitance.

UNIT – III

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation.

Text 1: 9.1, 9.1.1- 9.1.13 **10 Hrs**

Self Learning Components:

1. Understand the concept of EDIF and EDIF Syntax.
2. Discuss the the original "five-box" model of electrical connectivity.

UNIT – IV

Programmable ASIC logic cell, ASIC I/O cell A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation.

Text 1: 9.2, 9.4 **10 Hrs**

Self Learning Components:

1. Understand the concept half gate ASIC.
2. Define the term Synthesis and Simulation.

UNIT – V

ASIC Construction: System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow, global Routing, Detail Routing, Special Routing.

Text 1: 15.1- 15.4, 16.1.3, 16.1.5, 16.1.6, 16.2.4, 16.2.6, 16.2.8,16.3, 17.1, 17.2.17.3 **11 Hrs**

Self Learning Components:

1. Discuss the concept of FPGA Partitioning.
2. Understand the concept of Ratio-Cut Algorithm for Partitioning.

TEXT BOOK:

1. "**Application - Specific Integrated Circuits**", M.J.S .Smith, Pearson Education Publisher, 1st edition, ISBN-13: 978-8177584080, 2003.

REFERENCE BOOKS:

1. **"Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing"** Jose E.France, Yannis Tsividis, 2nd edition**,** Prentice Hall, ISBN-13: 978-0132036399, 1994.
2. **"Analog VLSI Design – NMOS and CMOS",** Malcolm R.Haskard; Lan. C. May, Prentice Hall, 1st edition, ISBN-13: 978-0130326409, 1998.

Professional Elective-II			
Course Title: **Multicore Architecture and Programming**			
Course Code: **P20MECE152**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the knowledge of Multi– core Architecture and System Overview of Threading.
2. Cover Fundamental Concepts of Parallel Programming and its Constructs.
3. Describe in detail the concepts of Threading APIs.
4. Explain the different aspects of OpenMP.
5. Cover Parallel Programming using OpenMP

B. Course Content

UNIT – I

Introduction to Multi– core Architecture: Motivation for Concurrency in software, Parallel Computing Platforms, Parallel Computing in Microprocessors, Differentiating Multi–core Architectures from Hyper– Threading Technology, Multithreading on Single–Core versus Multi–Core Platforms Understanding Performance, Amdahl's Law, Growing Returns: Gustafson's Law. System Overview of Threading: Defining Threads, System View of Threads, Threading above the Operating System, Threads inside the OS, Threads inside the Hardware, What Happens When a Thread Is Created, Application Programming Models and Threading, Virtual Environment: VMs and Platforms, Runtime Virtualization, System Virtualization.

Text 1: Chapters 1 and 2 **11 Hrs**

Self Learning Components:

Read and understand "Multi-Core Processors: New Way to Achieve High System Performance" Proceedings of the International Symposium on Parallel Computing in Electrical Engineering (PARELEC'06)

UNIT – II

Fundamental Concepts of Parallel Programming: Designing for Threads, Task Decomposition, Data Decomposition, Data Flow Decomposition, Implications of Different Decompositions, and Challenges You will Face, Parallel Programming Patterns. A Motivating Problem: Error Diffusion, Analysis of the Error Diffusion Algorithm. An Alternate Approach: Parallel Error Diffusion, Other Alternatives. Threading and Parallel Programming Constructs: Synchronization, Critical Sections,

Deadlock, Synchronization Primitives, Semaphores, Locks, Condition Variables, Messages, Flow Control–based Concepts, Fence, Barrier, Implementation dependent Threading Features.

Text 1: Chapters 3 and 4 **11 Hrs**

Self Learning Components:

Write a demo program in C language using open MP Library demonstrating Synchronization Primitives and Semaphores.

UNIT – III

OpenMP: A Portable Solution for Threading Challenges in Threading a Loop, Loop–carried Dependence, Data– race Conditions, Managing Shared and Private Data, Loop Scheduling and Portioning, Effective Use of Reductions, Minimizing Threading Overhead, Work–sharing Sections, Performance– oriented Programming, Using Barrier and No wait, Interleaving Single–thread and Multi– thread Execution, Data Copy–in and Copy–out, Protecting Updates of Shared Variables, Intel Task queuing Extension to OpenMP, OpenMP Library Functions, OpenMP Environment Variables, Compilation, Debugging, performance.

Text 1: Chapter 6 **10 Hrs**

Self Learning Components:

Write a demo program in C language using open MP Library demonstrating Single– thread and Multi– thread Execution,

UNIT – IV

Solutions to Common Parallel Programming Problems: Too Many Threads, Data Races, Deadlocks, and Live Locks, Deadlock, Heavily Contended Locks, Priority Inversion, Solutions for Heavily Contended Locks, Non–blocking Algorithms, ABA Problem, Cache Line Ping–ponging, Memory Reclamation Problem, Recommendations, Thread–safe Functions and Libraries, Memory Issues, Bandwidth, Working in the Cache, Memory Contention, Cache related Issues, False Sharing, Memory Consistency, Current IA– 32 Architecture, Itanium Architecture, High–level Languages, Avoiding Pipeline Stalls on IA–32, Data Organization for High Performance.

Text 1: Chapter 7 **10 Hrs**

Self Learning Components:

Reading and understanding a white paper on any Recent Multicore architecture

UNIT – V

Why Parallel Computers, Shared-Memory Parallel Computers, Programming SMPs and the Origin of OpenMP, What Is OpenMP?, Creating an OpenMP Program, The Bigger Picture, Parallel Programming Models, Ways to Create Parallel Programs, A Simple Comparison. **Overview of OpenMP:** Introduction The Idea of OpenMP, The Feature Set, OpenMP Programming Styles, Contents Correctness Considerations, erformance Considerations, **Writing a First OpenMP Program:** Introduction Matrix Times Vector Operation Using OpenMP to Parallelize the Matrix Times Vector Product Keeping Sequential and Parallel Programs as a Single Source Code. **OpenMP Language Features:** Introduction Terminology Parallel Construct Sharing the Work among Threads in an OpenMP Program Clauses to Control Parallel and Work-Sharing Constructs OpenMP Synchronization Constructs Interaction with the Execution Environment More OpenMP Clauses Advanced OpenMP Constructs

Text 2: Chapter 1, 2, 3 and 4 **10 Hrs**

Self Learning Components:

Writing C program using Open MP library and numerical analysis algorithm and demonstrate reduction in execution time as function of number of cores used.

TEXT BOOKS:

1. **"Multicore Programming, Increased Performance through Software Multi–threading",** Shameem Akhter and Jason Roberts, Intel Press, ISBN 0-9764832-4-6, 2006.
2. **"Using OpenMP, Portable Shared Memory Parallel Programming",** Barbara Chapman, Gabriele Jost, Ruud van der Pas, MIT Press, Massachusetts Institute of Technology, ISBN 978-0-262-53302, 2008.

REFERENCE BOOKS:

1. **"Principles of Parallel Programming"** Calvin Lin, Lawrence Snyder, Pearson Education, ISBN-13: 978-0321487902, 2009.
2. **"Parallel Programming in C with MPI and OpenMP"**, Michael J. Quinn**,** Tata McGraw Hill, ISBN 13: 9780070582019, 2004.
3. **"Parallel Computer Architecture A Hardware/ Software Approach"**, David E, Culler, Jaswinder Pal Singh with Anoop Gupta, eBook ISBN: 9780080573076 Hardcover ISBN: 9781558603431.

Professional Elective-II			
Course Title: **MEMS and Sensors**			
Course Code: **P20MECE153**	Semester: **I**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand the overview of microsystems, their fabrication and application areas.
2. Teach working principles of several MEMS devices.
3. Develop mathematical and analytical models of MEMS devices.
4. Understand the methods to fabricate MEMS devices.
5. Expose the students to various application areas where MEMS devices can be used.

B. Course Content

UNIT – I

Introduction: Why Miniaturization, Microsystems Versus MEMS, Why Microfabrication, Smart Materials, Structures and Systems, Integrated Microsystems, Applications of Smart Materials and Microsystems,

Micro Sensors, Actuators, Systems and Smart Materials: **An Overview:** Silicon Capacitive Accelerometer, Piezoresistive Pressure Sensor, Conductometric Gas Sensor, Fiber-Optic Sensors, Electrostatic Comb-Drive, Magnetic Microrelay, Microsystems at Radio Frequencies, Portable Blood Analyzer, Piezoelectric Inkjet Print Head, Micromirror Array for Video Projection, Micro-PCR Systems, Smart Materials and Systems.

Text 1: Chapter 1 and 2 **11 Hrs**

Self Learning Components:

Summary of the microfabrication and Micro sensors.

UNIT – II

Micromachining Technologies: Silicon as a Material for Micromachining, Thin-film Deposition, Lithography, Doping the Silicon Wafer: Diffusion and Ion Implantation of Dopants, Etching, Dry Etching, Silicon Micromachining, Specialized Materials for Microsystems.

Text 1: Chapter 3 **10 Hrs**

Self Learning Components:

Advanced Micro fabrication Processes.

UNIT – III

Mechanics of Slender Solids in Microsystems: The Simplest Deformable Element: A Bar, Transversely Deformable Element: A Beam, Energy Methods for Elastic Bodies, Examples and Problems, Heterogeneous Layered Beams, Bimorph Effect, Residual Stresses and Stress Gradients, Poisson Effect and the Anticlastic Curvature of Beams, Torsion of Beams and Shear Stresses, Dealing with Large Displacements, In-Plane Stresses, Dynamics.

The Finite Element Method: Need for Numerical Methods for Solution of Equations, Variational Principles, Weak Form of the Governing Differential Equation, Finite Element Method, Numerical Examples, Finite Element Formulation for Time-Dependent Problems, Finite

Element Model for Structures with Piezoelectric Sensors and Actuators, Analysis of a Piezoelectric Bimorph Cantilever Beam.

Text 1: Chapter 4 and 5 **11 Hrs**

Self Learning Components:

Study on Integrated Microsystems.

UNIT – IV

Modeling of Coupled Electromechanical Systems: Electrostatics, Coupled Electromechanics: Statics, Coupled Electromechanics: Stability and Pull-In Phenomenon, Coupled Electromechanics: Dynamics, Squeezed Film Effects in Electromechanics, Electro-Thermal-Mechanics, Coupled Electromagnet-Elastic Problem.

Text 1: Chapter 6 **10 Hrs**

Self Learning Components:

Case Study on Smart Structure in Vibration Control.

UNIT – V

Electronics Circuits and Control for Micro and Smart Systems: Semiconductor Devices, Electronics Amplifiers, Signal Conditioning Circuits, Practical Signal conditioning Circuits for Microsystems, Introduction to Control Theory, Implementation of Controllers.

Integration of Micro and Smart Systems: Integration of Microsystems and Microelectronics, Microsystems Packaging, Mechanisms.

Text 1: Chapter 7 & 8.1-8.2 **10 Hrs**

Self Learning Components:

Case Study on Smart system.

TEXT BOOK:

1. **"Micro and Smart Systems",** Dr. A.K.Aatre, Ananth Suresh, K.J.Vinoy, S. Gopalakrishna, K.N.Bhat., John Wiley Publications, 2002, ISBN: 1118213904, 9781118213902 2.

REFERENCE BOOKS:

1. **"MEMS & Microsystems: Design and Manufacture",** Tai-Ran Tsu, Tata Mc-Graw-Hill.2002.8th reprint, ISBN-13:978-0-07-048709-3. ISBN-10:0-07-048709-X
2. **"RF MEMS Theory, Design and Technology"** GABRIEL M. REBEIZ. 2003 A John Wiley & Sons Publication. ISBN: 978-0-471-20169-4 4.
3. **"Microsystems Design",** S. D. Senturia, Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-79237246-8.

VIDEO LECTURE:

1. **https://nptel.ac.in/courses/117/105/117105082/#watch** Lectured by Prof. Santiram Kal, IIT Kharagpur.

Laboratory --I			
Course Title: **VLSI and Embedded System Laboratory - I**			
Course Code: **P20MECEL16**	Semester: **I**	L-T-**P-H** : 0-0-**4-4**	Credits:**2**
Contact Period : Lab: **36 Hrs**.; Exam: **3 Hrs**.		Weightage: CIE: **50 %**	SEE: **50%**

A. Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to:

1. Understand the basic knowledge of how to use CADENCE Tool for VLSI concepts.
2. Analyze the ASIC Design flow.
3. Design and Verify Basic/universal gates using verilog code.
4. Design and Verify combinational and sequential circuits.
5. Design and Verify a testing program for specified conditions using multithread application.
6. Design a POSIX based message queue for communicating between two tasks as per the requirements specified.

B. Course Content

A.**VLSI Digital Design**

1. Write Verilog Code for the following circuits and their Test Bench for verification,
   - An inverter, Buffer and Transmission gate
   - Basic/Universal gates
   - Flip flop -RS, D, JK, MS, T
2. Write Verilog code for the following circuits and their Test Bench for verification
   - Carry Ripple Adder
   - Carry LookAhead adder
   - Carry Skip Adder

ASIC-Digital Design Flow

Design the following circuits

3. Write a Verilog Code for 8-bit Booth Multiplication (Radix-4)
4. Write Verilog code for 4/8-bit Magnitude Comparator, Parity Generator,
5. Write Verilog code for 4/8-bit, LFSR, Universal Shift Register
6. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.

B. Embedded Programming Concepts (RTOS)

1. Create ‘n’ number of child threads. Each thread prints the message “ I’m in thread number ” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
2. Implement the multithread application satisfying the following:
   i. Two child threads are crated with normal priority.
   ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
   iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.
3. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.
4. Test the program below using multithread application.

i. The main thread creates a child thread with default stack size and name 'Child_Thread'.
ii. The main thread sends user defined messages and the message 'WM_QUIT' randomly to the child thread.
iii. The child thread processes the message posted by the main thread and quits when it receives the 'WM_QUIT' message.
iv. The main thread checks the termination of the child thread and quits when the child thread complete its execution.
v. The main thread continues sending the random messages to the child thread till the 'WM_QUIT' message is sent to child thread.
vi. The messaging mechanism between the main thread and child thread is synchronous.

5. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the 'Read Handle' of the pipe to a second process using memory mapped object. The first process writes a message 'Hi from Pipe Server'. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.
6. Create a POSIX based message queue for communicating between two tasks as per the requirements given below:-
   i. Use a named message queue with name 'MyQueue'.
   ii. Create two tasks (Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   iii. Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   iv. Task2 open the message queue and posts the message 'Hi from Task2'. Handle all possible error scenarios appropriately.

TEXT BOOKS:

1. **"Introduction to Embedded Systems",** Shibu K V, TMH Education Pvt Ltd, Second reprint, 2010, ISBN(13): 978-0-07-014589-4.
2. **"Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology: Circuit Design, and Process Technology"** Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, CRC Press, ISBN-10: 0-8493-7924-5, ISBN-13: 978-0-8493-7924-6, 2006.

REFERENCE:

1. "**Digital VLSI Design (RTL to GDS)**" Dr. Adam Teman , Emerging nanoscaled Integrated Circuits and Systems (EnICS) Labs Faculty of Engineering, Bar-Ilan University https://www.youtube.com/watch?v=RbZ3BXbd6_k&list=PLZU5hLL_713x0_AV_rVbay0pWmED7992G
2. https://www.vlsisystemdesign.com/Clock-Tree-Synthesis-Video-Series.php
3. https://www.udemy.com/course/vlsi-academy-physical-design-flow/

Course Title: **CMOS Mixed Mode VLSI Circuits**			
Course Code: **P20MECE21**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the knowledge about basics of high speed IC design.
2. Cover basic current reference circuits.
3. Familiarize CMOS amplifiers design.
4. Explain the working of switched capacitor circuit.
5. Cover Designing of high speed Data converters

B. Course Content

UNIT – I

MOS Transistors: Transistor structure, characteristics of MOS transistors, Drain current in the strong inversion approximation, Drain current in the sub threshold region, MOS transistor capacitances, Scaling effects on MOS transistors, Transistor SPICE models, Electrical characteristics, Temperature effects, Noise models.

Physical Design of MOS IC's: MOS Transistors, Passive components, Capacitors, Resistors, Inductors, Integrated-circuit (IC) interconnects, Physical design considerations, IC packaging.

Text 1: Chapters 2 and 3 **11 Hrs**

Self Learning Components:

Study at least 2 spice models for P-MOS and N-MOS transistors and plot Output characteristics using those SPICE models with the help of any simulator

UNIT – II

Basic Current Reference Circuits: Current mirrors, Simple current mirror, Cascode current mirror, Low-voltage active current mirror, Current and voltage references, Supply-voltage independent current reference, Bandgap references, Low-voltage bandgap voltage reference, Curvature-compensated bandgap voltage reference, Floating-gate voltage reference.

CMOS Amplifiers: Differential amplifier, Linearization techniques for transconductors, Single-stage amplifier, Folded-cascode amplifier.

Text 1: Chapters 4 and 5 **10 Hrs**

Self Learning Components:

Design and Simulate current mirrors in CAD tool. Understanding the requirements of Op-Amps and their implications on design by referring different vendors' product data sheets

UNIT – III

CMOS Amplifiers: Fully differential amplifier architectures, Multi-stage amplifier structures, Rail-to-rail amplifiers, Amplifier characterization.

Non-Linear Analog Components: Comparators, Multipliers.

Text 1: Chapters 5 and 6 **10 Hrs**

Self Learning Components:

Design and simulate a single stage /differential amplifier for given requirements across different technologies, note the limitations and benefits.

UNIT – IV

Switched Capacitor Circuits: Anti-aliasing filter, Capacitors, Switches, Programmable capacitor arrays, Operational amplifiers, Track-and-hold (T/H) and sample-and-hold (S/H) circuits, Switched-capacitor (SC) circuit principle, SC filter design, SC ladder filter based on the LDI transform, SC ladder filter based on the bilinear transform, Effects of the amplifier finite gain and bandwidth, Settling time in the integrator, Amplifier dc offset voltage limitations, Computer-aided analysis of SC circuits, Computer-aided analysis of SC circuits, Circuit structures with low sensitivity to nonidealities, Low-voltage SC circuits.

Text 1: Chapter 8 **10 Hrs**

Self Learning Components:

To study and understand "Dynamic analog resonator-based adaptive filters". ISCAS 2000: 161-164 IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland.

UNIT – V

Data Converter Principles: Binary codes, Data converter characterization. **Nyquist Digital-to-Analog Converters:** Digital-to-analog converter (DAC) architectures, Voltage-scaling DACs, Current-scaling DACs, Charge-scaling DAC, Hybrid DAC, Configuring a unipolar DAC for the bipolar conversion, Algorithmic DAC. **Nyquist Analog-to-Digital Converters:** Analog-to-digital converter (ADC) architectures Successive approximation register ADC, Integrating ADC

Text 1: Chapters 9, 10, 11 **11 Hrs**

Self Learning Components:

To study IEEE Transaction article "A high-frequency double-sampling second-order Delta Sigma modulator" and simulate any functional block.

TEXT BOOK:

1. **"CMOS Analog Integrated Circuits High-Speed and Power-Efficient Design",** Tertulien Ndjountche, CRC Press, ISBN: -13: 978-1-138-59972-7, 2019.

REFERENCE BOOKS:

1. **"Design of Analog CMOS Integrated Circuits**", Behzad Razavi, Tata McGraw Hill, 1st edition, ISBN 0-07-238032-2, 2008.
2. **"CMOS Analog Circuit Design",** Phillip E. Allen, Douglas R.Holberg, Oxford University Press, 3rd edition, ISBN: 9780199765072, 2011.
3. **"CMOS Circuit Design, Layout and Simulation",** R. Jacob Baker,Harry W. Li, David E. Boyce, Prentice Hall of India, 1st edition, ISBN-13: 978-0780334168 ISBN-10: 0780334167, 2005.

Course Title: **Low Power VLSI Design**			
Course Code: **P20MECE22**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand the ttypes of power dissipation in CMOS devices.
2. Discuss different techniques of power analysis and digital cell library.
3. Discuss the concepts of Low power Clock Distribution.
4. Design low power arithmetic circuits and systems
5. Understand the architecture and performance management of the system.

B. Course Content

UNIT – I

Introduction: Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Basic Principles of Low Power Design Low Power Figure of Merits.

Simulation Power Analysis: SPICE Circuit Simulation, Discrete Transistor Modeling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis

Text 1:1.1-1.4, 2.1-2.4, **10 Hrs**

Self Learning Components:

1. Understand the influence of Static Current in power analysis.
2. Understand how the Data Correlation Analysis in done in DSP Systems.

UNIT – II

Probabilistic Power Analysis: Random Logic Signals, Probability and Frequency, Probabilistic Power Analysis Techniques.

Circuit: Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Adjustable Device Threshold Voltage

Text 1:3.1-3.3, 4.1- 4.3, 4.6. **11 Hrs**

Self Learning Components:

1. Discuss the concept of Signal Entropy
2. Discuss the concept of Low Power Digital Cell Library.

UNIT – III

Low Power Circuit Techniques: Introduction, Power Consumption in Circuits, Flip-flops and Latches, Logic.

Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver vs. Distributed Buffers**,** Buffer and Device Sizing under Process Variations, Zero Skew vs. Tolerable Skew

Text 2: 3.1- 3.4, 5.1- 5.4. . **11 Hrs**

Self Learning Components:

1. Understand the concept of High Capacitance Nodes.
2. Explain how the Chip and Package Co-Design of Clock Network is done.

UNIT – IV

Low Power Arithmetic Components: Introduction**,** Circuit Design Style**,** Adders, Multipliers.
Low Power Memory Design: Introduction, Sources and Reductions of Power Dissipation in Memory Subsystem, Sources of Power Dissipation in DRAM and SRAM, Low Power DRAM Circuits.
Text 2: 7.1- 7.4, 8.1 - 8.4. **10 Hrs**
Self Learning Components:

1. Understand the concept of division in low power arithmetic components.
2. Compare the features of Low Power SRAM and DRAM Circuits.

UNIT – V

Architecture and System: Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Operator Reduction.
Advanced Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous System Basics.
Text 1: 7.1-7.4.1, 8.1-8.3.1. **10 Hrs**
Self Learning Components:

1. Understand the concept of Loop Unrolling.
2. Understand the concept of Prospects of Asynchronous Computation.

TEXT BOOKS:

1. **"Practical Low Power VLSI Design"**, Gary K, Yeap, Kluwer Academic Publishers, ISBN – 13**:** 978-0792380092, 2008,
2. **"Low Power Design Methodologies"** Rabaey, Pedram**,** Kluwer Academic Publishers, ISBN – 978-1-4613-5975-3, 2009.

REFERENCE BOOKS:

1. **"Low Power Low Voltage VLSI Subsystem"** Kiat Seng Yeo and Kausik Roy**,** Tata Mc Gram Hill. ISBN- 9780071437868, 2005.
2. **"Designing CMOS Circuits for Lower Power"** Soudris D, Piguet C and Goutis C, Kluwer Academic Publishers, ISBN -9781402072345, 2002.

Course Title: **Automotive Electronics Design Fundamentals**			
Course Code: **P20MECE23**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide an insight into electronics used with Automobiles
2. Provide a basic understanding of engine operation
3. List and analyze different sensors used in Automotive electronics
4. Discuss basic design of different electronics blocks at various abstract levels
5. Do a case study to understand practical implementation of Automotive electronics
6. Equip student with methodology to design electronics system needed in automobile
7. Explore communication technologies used in automobile

B. Course Content

UNIT – I

Introduction: Motivation for electronic engine control, The role of electronics, Concept of an electronic engine control system, Definition of engine performance terms.

Instrument Cluster, Heating and Cooling, Airbag Safety, Antilock Brake, Traction and Stability, Power Assist Steering, Avionics Fly-By-Wire (FBW) , Automotive X- By-Wire, Tire Pressure Monitoring, Modules Count

Straight-Wire-Switch Topology, Embedded Function, A Conventional Radio, An Embedded Radio, Distributed Vehicle Architecture, Custom Built Modules, Modules Cross Compatibility, Integrating Dissimilar Functions, Integrating Identical Functions: A Universal Module, Key-Off Load Current, 12V/42V Electrical Supply System, Vehicle Input Sensors and Switches, Vehicle Output Devices, Vehicle Interior Lights Dimming,

H-Bridge Motor Driver, Communication Link, Vehicle Programming, Vehicle Operating Software, High Level Software Context Diagram

Text 1: Chapter 5 (selected articles)

Text 2: Chapter 1(selected articles) **10 Hrs**

Self Learning Components:

1. Parameters influencing performance of an Automobile
2. Case Study Nissan Quest., Mini Van Modules

UNIT – II

Sensors in Automobiles: Automotive Control System Applications of Sensors, Throttle Angle Sensor, Temperature Sensors, Typical Coolant Sensor, Sensors for Feedback Control, Knock Sensors, Angular Rate Sensor, LIDAR, Digital Video Camera, Flex-Fuel Sensor

Text 1: Chapter 6 (selected articles) **10 Hrs**

Self Learning Components:

1. Study the data sheet of sensors used in Automobiles (ref: Internet)
2. List the actuators used in Automobiles (ref: Text 1)

UNIT – III

Fundamentals Module Blocks and Topology: Fundamentals Module Blocks: Introduction, Module Hardware Blocks: The Safety and Protection, The Switched Battery, The Power Reservoir, The Power Supply, The Ignition Switch, Start Interface, The Ignition Switch Run, Input Interface Circuits, The Processing Power, Reset and Watch Dog Timer, Reset and Watch Dog Timer, The Program Storage, The Critical Data Storage, The Flash Programming Port, Specific Function Drivers, Communication Node, Module Software Blocks: Application Software, Primary Boot Loader, The Real Time Operating
System (RTOS),The Network Operating System (NOS), Vehicle Interface: Vehicle Alternator, 20A Relays and Solenoids, 20B Battery, and 20D Starter Motor, Vehicle Specific Input Functions, Vehicle Ignition Switch, Vehicle Specific Output Functions, Vehicle Modules, Diagnostics Connector

Fundamental Block Module Topology: Introduction, Safety and Protection, Power Supply Battery Power Switching, Sensor Power Switching, Ignition Switch Interface, Input Interface Architecture, Specific-Function Driver, Low-Side Driver, Pulse Width Modulated Driver, Watch Dog Timer, Reset Topology, Digital Communication Architecture, CAN Communication Node Architecture, CAN Protocol Controller, Controller Area Network Transceiver, CAN Bus Implementation Strategies, CAN Bus Voltage Levels, CAN Bus Software Components,
Battery Voltage Monitoring, Abrupt Power Failure. Power delivery and Functional attributes: Power delivery mechanism, Type 1 & 2 modules operation, Type 2 modules vehicles life, Module functional attributes.

Text 2: **Chapter 2, 3, 4** **11 Hrs**

Self Learning Components:

1. Study Vehicle communications and prepare a report (Ref: Chap 9 of Text 1)

UNIT – IV

Fundamental Block Design: Introduction, Battery Switching Block Definition, Ignition Start Sensing Block Definition, Sensors Power Switching Block Definition, Low-Side Output Device Driver, High-Side Output Device Driver, Input Signal Senor Block, Reset Block, Reverse Battery, Power Supply Block

Text 2: **Chapter 5** **11 Hrs**

Self Learning Components:

1. Lincoln Motor Company: Case Study 2015 Lincoln—MK*C* (Ref: Chap 6 of text 2)

UNIT – V

Vehicle Communication and Safety: IVN, Local Interconnect Network, FlexRay IVN, MOST IVN, MOST IVN ,Vehicle to Infrastructure Communication, Vehicle-to-Cellular Infrastructure, Quadrature Phase Shifter and Phase Modulation (QPSR), Short-Range Wireless Communications ,Satellite Vehicle Communication ,GPS Navigation Airbag Safety Device ,Blind Spot Detection ,Automatic Collision Avoidance System ,Lane Departure Monitor
Tire Pressure Monitoring System, Enhanced Vehicle Stability

Text 2: **Chapter 9, 10** **10 Hrs**

Self Learning Components:

1. Case Study: Safety and communication features in any four brand of cars (refer: Data sheet of manufacturer)

TEXT BOOKS:

1. **"Understanding Automotive Electronics" -** William B. Ribbens, 8th edition, Elsevier (B H) publications, ISBN: 978-0-12-810434-7, 2017
2. **"Automotive Electronics Design Fundamentals"**, Najamuz Zaman, Springer International, ISBN 978-3-319-17583-6, 2015.

REFERENCE BOOKS:

1. **"Bosch Automotive Electrics and Automotive Electronics"** Springer International, ISBN 978-3-658-01784-2, 2014,
2. **"Fundamentals of Automotive Electronics"**- V A W Hillier, 2nd edition Nelson Thrones, ISBN 0 7487 2695 0
3. **"Automotive Electronics Handbook"** Ronald K. Jurgen, 2nd edition, McGraw Hill, ISBN-13: 978-0070344532.

Professional Elective-III			
Course Title: **ARM Processors**			
Course Code: **P20MECE241**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand general architecture of ARM processor
2. Thoroughly discuss architecture of Cortex family M3 & M4 Processors
3. Implement embedded systems using Cortex M3 & M4
4. Debug faults in the Cortex M3 & M4 processor based systems
5. Highlight specialities of Cortex M3 & M4 processors
6. Choose processor based on the system specifications

B. Course Content

UNIT – I

Introduction to Cortex M Processors: Introduction to ARM Cortex M processors, Introduction Embedded Software Development Technical Overview.

Text1: Chapter 1, 2, and 3 **10 Hrs**

Self Learning Components:

1. Survey the different versions of ARM processors and make a comparison of their features

UNIT – II

Architecture and Memory Systems: Introduction to the Architecture: Architecture, Programmer's model, Behavior of the application program status register (APSR), Memory system, Exceptions and interrupts

Memory systems: Overview of memory system features ,Memory map, Connecting the processor to memory and peripherals ,Memory requirements, Memory endianness , Data alignment and unaligned data access support ,

Bit-band operations, Default memory access permissions, Memory access attributes, Memory system in a microcontroller.

Text 1: Chapter 4 and 6 **11 Hrs**

Self Learning Components:

1. Study the instruction set of Cortex M Processors (ref Chap 5 of text 1)

UNIT – III

Exceptions and Interrupts: Overview of exceptions and Exception types, Overview of interrupt management, Definitions of priority, Vector table and vector table relocation, Interrupt inputs and pending behaviors, Exception sequence overview , Details of NVIC registers for interrupt control, Details of SCB registers for exception and interrupt control , Details of special registers for exception or interrupt masking.

Interrupt latency and exception handling optimization,

Text 1: Chapter 7 and 8 **11 Hrs**

Self Learning Components:

1. Develop a program to demonstrate use of interrupts and exceptions

UNIT – IV

Low Power and System Control Features: Low power designs, Low power features, Using WFI and WFE instructions in programming, Developing low power applications, The SysTick timer, Self-reset, CPU ID base register, Configuration control register, Auxiliary control register, Co-processor access control register

Memory Protection Unit (MPU): Overview of the MPU, MPU registers, Setting up the MPU, Memory barrier and MPU configuration, Using sub-region disable, Considerations when using MPU, Other usages of the MPU

Text1: **Chapter 9 and 11** **10 Hrs**

Self Learning Components:

1. List the low power features of all Cortex series processors

UNIT – V

Fault Exceptions and Fault Handling: Overview of fault exceptions, Enabling fault handlers, Fault status registers and fault address registers, Analyzing faults, Faults related to exception handling, Lockup, Fault handlers

Introduction to the Debug and Trace Features: Debug and trace features overview, Debug architecture, Debug modes, Debug events, Breakpoint feature, Debug components introduction, Debug operations.

Text 1: **Chapter 12 and 14** **10 Hrs**

Self Learning Components:

1. Study the software porting from 8/16 bit controllers to Cortex M processors (ref chap 24 of Text 1)

TEXT BOOK:

1. **"The Definitive Guide to ARM CortexM3 and Cortex-M4 Processors"**, Joseph Yiu, 3rd edition , Newness publications, ISBN 13: 978-0-12-408082-9, 2016**.**

REFERENCE BOOKS:

1. **"ARM System –On-Chip-Architecture"**, Steve Furber, 2nd edition , Addison Wesley, ISBN 10: 0201675196 / ISBN 13: 9780201675191.
2. **"ARM System Developer's Guide: Designing and Optimizing System Software"**, Andrew Sloss, Dominic Symes, Chris Wright, Elsevier Morghan Kaufmann publishers ISBN 1-55860-874-5.

Professional Elective-III			
Course Title: **Embedded System Design With FPGA**			
Course Code: **P20MECE242**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provides basic knowledge of embedded system.
2. Explain the computer hardware and software.
3. Illustrate the concept of the SAYEH Design and Test.
4. Describe the concept of Field Programmable gate arrays.
5. Explain the embedded system design tools and design prototyping.
6. Describe the various concept of design of utility hardware cores.
7. Explain the concepts of embedded design steps.

B. Course Content

UNIT – I

Computer Hardware and Software: Computer System, Computer Software, Machine Language, Assembly Language, High-Level Language, C Programming Language, Instruction Set Architecture, SMPL-CPU Design, CPU Specification, Single-Cycle Implementation, Multi-Cycle Implementation, SAYEH Design and Test, Details of Processor Functionality, SAYEH Datapath, SAYEH Verilog Description, SAYEH Top-Level Testbench / Assembler.

Text 1: Chapter 4 **10 Hrs**

Self Learning Components:

SAYEH Hardware Realization.

UNIT – II

Field Programmable Devices: Read Only Memory, Basic ROM Structure, NOR Implementation, Distributed Gates, Array Programmability, Memory View, ROM Variations, Programmable Logic Arrays, PAL Logic Structure, Product Term Expansion, Three-State Outputs, Registered Outputs, Commercial Parts, Complex Programmable Logic Devices, Altera's MAX 7000S CPLD, Field Programmable gate arrays, Altera's FLEX 10K DOGMA, Altera's cyclone DOGMA.

Text 1: Chapter 5 **10 Hrs**

Self Learning Components:

Altera's cyclone DOGMA.

UNIT – III

Tools For Design and Prototyping: Hardware Design Flow, Datapath of Serial Adder, Serial Adder Controller, HDL Simulation and Synthesis, Pre-Synthesis Simulation, Module Synthesis, Post-Synthesis Simulation, Mixed-Level Design with Quartus II, Project Specification, Block Diagram Design File, Creating and Inserting Design Components, Wiring Design Component, Design Compilation, Design Simulation, Synthesis Results, Design Prototyping, UP3 Board Specification, DE2 Board Specification .

Text 1: Chapter 6 **10 Hrs**

Self Learning Components:
Programming DE2 Cyclone II.

UNIT – IV

Design of Utility Hardware Cores: Library Management, Basic IO Device Handling, Debouncer, Single Stepper, Utilizing UPS Basic IO, Utilizing DE2 Basic IO, Frequency Dividers, Seven Segment Displays, SSD Driver, Testing DE2 SSD Driver, LCD Display Adapter, Writing into LCD, LCD Initialization, Display Driver with Initialization, Testing the LCD Driver (UPS), Testing the LCD Driver (DE2), Keyboard Interface Logic, Serial Data Communication, Power-On Routine, Codes and Commands, Keyboard Interface Design, VGA Interface Logic, VGA Driver Operation, Monitor Synchronization Hardware, Character Display, VGA Driver for Text Data, VGA Driver Prototyping (UPS),.

Design with Embedded Processors: Embedded Design Steps, Processor Selection, Processor Interfacing, Developing Software, Filter Design, Filter Concepts, FIR Filter Hardware Implementation, FIR Embedded Implementation, Building the FIR Filter, Design of a Microcontroller, System Platform.

Text 1: Chapter 7 and 8 **11 Hrs**

Self Learning Components:
VGA Driver Prototyping (DE2), Microcontroller Architecture.

UNIT – V

Design Of An Embedded System: Designing an Embedded System, Nios II Processor, Configurability Features of Nios II, Processor Architecture, Instruction Set,Nios II Alternative Cores, Avalon Switch Fabric, Avalon Specification, Address Decoding Logic, Data-path Multiplexing, Wait-state Insertion, Pipelining, Endian Conversion, Native Address Alignment and Dynamic Bus Sizing, Arbitration for Multi-Master Systems, Burst Management, Clock Domain Crossing, Interrupt Controller, Reset Distribution, SOPC Builder Overview, Architecture of SOPC Builder Systems, Functions of SOPC Builder, IDE Integrated Development Environment, IDE Project Manager, Source Code Editor, C/C++ Compiler, Debugger , Flash Programmer, An Embedded System Design: Calculator, System Specification, Calculating Engine, Calculator IO interface. **11 Hrs**

Text 1: Chapter 9

SLC: Design of Calculating Engine, Building Calculator Software, Calculator Program, Completing the Calculator System.

TEXT BOOK:

1. **"Embedded Core Design with FPGAs"**, Zainalabedin Navabi, 1st edition, McGraw Hill, ISBN-10: 0070139784, ISBN-13: 978-0070139787, 2008.

Professional Elective-III			
Course Title: **Robotics and Automation**			
Course Code: **P20MECE243**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. To familiarize students with brief history of robot and basic concepts of industrial robot.
2. To expose the students to kinematics of robots and programming of robot
3. To study the trajectory planning for robot
4. To study the Euler, Lagrangian formulation of Robot dynamics
5. To make the students familiar with various applications in robots in industry

B. Course Content

UNIT – I

Introduction: Industrial Automation and Computers, Industrial Robot, Robot Population and Application, Do Robots Create More Unemployment?, Payback Period of a Robot, Robot Applications in Manufacturing

Grippers and Tools of Industrial Robot: Introduction, Definitions of Industrial Robot, Configuration and Work Volume, Precision of Movement, Degrees of Freedom, End Effectors.

Coordinate Transformation: Introduction, 2D Coordinate Transformation, Description of Object, 3D Coordinate Transformation, Inverse Transformation, Composite Transformation Matrix, The Wrist.

Text 1: Chapter 1, 2, 3 **11 Hrs**

Self Learning Components:

1. Understand the coordinate frames and transformations using Robo Analyser.

UNIT – II

Kinematics: Introduction, Joint Coordinate Space, Kinematics and Inverse Kinematics, Link Parameters, D-H Notation of Coordinate Frames, D-H Transformation Matrix, Symbolic Procedure, D-H Algorithm, Application Examples, Jacobian.

Text 1: Chapter 4 **10 Hrs**

Self Learning Components:

1. Forward/Inverse kinematics and validation using software (Robo Analyser/MathLab or any other free software tool).

UNIT – III

Robot Sensors: Introduction, Internal and External Sensors, Applications of Robot Sensors, Desirable Features of Robot Sensors, Proximity and Tactile Sensors, Range Sensors, Force Sensors, Vision System for Inspection.

Robot Control: Introduction, Euler–Lagrange Equation, Joint Motion, Second-Order Systems, State-Space Equations, Lyapunov Stability, Lyapunov First Method, Lyapunov Second Method, Control Unit, Electric, Hydraulic and Pneumatic Drives, Industrial Vision System, Inspection Using Industrial Vision, Camera

Text 1: Chapter 5, 6 **11 Hrs**

Self Learning Components:

1. Denavit-Hartenberg (DH) parameter validation using a Robo Analyser software.

UNIT – IV

Robot Programming and Work Cell: Introduction, Language Structure, Robot Programming Languages, Robot Motion, SCORBOT-ER, Sensor Integration, Robot Work Cell, Interference Problems, Interference Problems, Further on Robot Work Cell.

Robot Trajectory Planning: Introduction, Trajectory Planning Terminologies, Steps in Trajectory Planning, p-Degree Polynomial Trajectories, Linear Function with Parabolic Blends, Issues On LFPB Trajectories, Bang-Bang Trajectory, Cartesian Space Versus Joint Space.

Text 1: Chapter 7, 10 **10 Hrs**

Self Learning Components:

1. Integration of assorted sensors (IR, Potentiometer, strain gages etc.) to micro controllers

UNIT – V

Robot Dynamics: Introduction, Lagrangian Design, N-Link Robot Manipulator, Slender Rod as Robot Link.

Robot Applications: Robots in Industry, Robots in Handling, Compliance, Assembly, Injection Moulding.

Medical Applications of Robots: Classification of Medical Robots, Slow Growth, Rehabilitation Robots, Guide Robot, Guide Cane, Prosthetic Limb, Prosthetic Arms, Exoskeleton, Hospital Service Robot, Clinical Robot

Text 1: chapter 13, 9, 15 **10 Hrs**

Self Learning Components:

1. Industrial Robot programming using VAL II or equivalent / simpler laboratory version of robotic arm.

TEXT BOOK:

1. "**Introduction to Industrial Robotics**", Ramachandran Nagarajan, Pearson, ISBN 978-93-325-4480-2, eISBN 978-93-325-7872-2, 2016.

REFERENCE BOOKS:

1. **"Introduction to Robotics"**, S K Saha, 2nd edition McGraw Hill, ISBN (13): 978-93-3290-2800, ISBN (10): 93-3290-280-1, 2014.
2. **"Industrial Robots",** Michell Grover, Mitchel weiss, Roger nagel ,McGraw Hill, India ,2nd edition, ISBN-13:9780070265097, 2012.
3. **"Robotics",** K.S. Fu, R.C. Gonzales and Lee, McGraw Hill Intl. India, 1st edition, ISBN-13:9780070265103, 2008
4. **"Robotics for Engineers",** Yoramn Koren,Mc Graw hill Intl. Book Co., New Delhi, ISBN-13:9780070353992, 1987.

Professional Elective-IV			
Course Title: **SystemVerilog for Design and Verification**			
Course Code: **P20MECE251**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the basic understanding of SystemVerilog operators, loops, jumps, functions
2. Explain the SystemVerilog data types and typedefs
3. Explain the SystemVerilog Class and Randomization.
4. Describe the Functional Coverage and advanced Interfaces.

B. Course Content

UNIT – I

Introduction to System Verilog: SystemVerilog origins, Key SystemVerilog enhancements for hardware design. **SystemVerilog Declaration Spaces:** Packages, $unit compilation-unit declarations, Declarations in unnamed statement blocks, Simulation time units and precision. **SystemVerilog Literal Values and Built-in Data Types:** Enhanced literal value assignments, define enhancements, SystemVerilog variables, Using 2-state types in RTL models, Relaxation of type rules, Signed and unsigned modifiers, Static and automatic variables, Deterministic variable initialization, Type casting.

Text 1: Chapter 1, 2, 3 **11 Hrs**

Self Learning Components:

1. Understand the Difference between Verilog and SystemVerilog.
2. Prepare the case study report on SystemVerilog Tools.

UNIT – II

SystemVerilog User-Defined and Enumerated Types: User-defined types: Enumerated types, **SystemVerilog Arrays, Structures and Unions:** Structures, Unions, Arrays, The for each array looping construct, Array querying system functions ,The $bits “size of” system function, Dynamic arrays, associative arrays, sparse arrays and strings.

Text 1: Chapter 4, 5 **10 Hrs**

Self Learning Components:

1. Understand the Uses of Enumerated types.
2. Write a verilog program by using strings.

UNIT – III

SystemVerilog Procedural Blocks, Tasks and Functions: Verilog general purpose always procedural block, SystemVerilog specialized procedural blocks, Enhancements to tasks and functions.

SystemVerilog Procedural Statements: New operators, Operand enhancements, Enhanced for loops, Bottom testing do while loop, the for each array looping construct, New jump statements — break, continue, return. Enhanced block names, Statement labels, Enhanced case statements, Enhanced if...else decisions.

Text 1: Chapter 6, 7 **10 Hrs**

Self Learning Components:

1. Discuss the SystemVerilog ATM example.
2. Understand the uses of Procedural Statements in writing the program.

UNIT – IV

Verification Guidelines: Introduction, The Verification Process, The Verification Plan, The Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, What Should You Randomize?, Functional Coverage, Testbench Components, Layered Testbench, Building a Layered Testbench ,Simulation Environment Phases , Maximum Code Reuse , Testbench Performance.

Data Types: Introduction , Built-in Data Types, Fixed-Size Arrays , Dynamic Arrays , Queues , Associative Arrays , Linked Lists , Array Methods , Choosing a Storage Type , Creating New Types with typedef , Creating User-Defined Structures , Enumerated Types , Constants , Strings , Expression Width ,Net Types.

Text 2: Chapter 1, 2 **11 Hrs**

Self Learning Components:

1. Understand the concept of Routine Arguments.
2. Discuss Where to Define a Class.

UNIT – V

Functional Coverage: Introduction , Coverage Types , Functional Coverage Strategies , Simple Functional Coverage Example , Anatomy of a Cover Group , Triggering a Cover Group , Data Sampling , Cross Coverage , Coverage Options , Parameterized Cover Groups , Analyzing Coverage Data , Measuring Coverage Statistics During Simulation

Advanced Interfaces: Introduction, Virtual Interfaces with the ATM Router, Connecting to Multiple Design Configurations, Procedural Code in an Interface.

Text 2: Chapter 9, 10 **10 Hrs**

Self Learning Components:

1. Understand the concepts of Composition, Inheritance, and Alternatives.
2. Understand the concepts of Semaphores, Mailboxes.

TEXT BOOKS:

1. **"SystemVerilog For Design: A Guide to Using SystemVerilog for Hardware Design and Modeling",** Stuart Sutherland Simon Davidmann Peter Flake, Spinger , 2nd edition, ISBN-10: 0-387-33399-1 e-ISBN-10: 0-387-36495-1
2. **"SystemVerilog for Verification a Guide to Learning the Testbench Language Features**", Chris Spear Synopsys, Inc., 2nd edition, ISBN 978-1-4419-4561-7 ISBN 978-0-387-76530-3 (eBook)

REFERENCE BOOKS:

1. **"SystemVerilog for Design",** Sutherland, 2nd edition Springer publications, ISBN 978-0-387-36495-7, 2006.
2. **"SystemVerilog Assertions",** Vijaya Raghavan, Springer publications, ISBN 978-1-4614-7324-4, 2014.

Professional Elective-IV			
Course Title: **Design of VLSI Systems**			
Course Code: **P20MECE252**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the basic knowledge of VLSI system design
2. Explain the concept of VLSI System Design Methodology and Chip Design Methods.
3. Provide the understanding of Design Capture Tools.
4. Highlight the concept of Data Path Sub System Design and Array Subsystem Design
5. Outline the concepts of Control Unit Design and Special Purpose Subsystems.
6. Provide the knowledge of Design Economics, VLSI System Testing & Verification

B. Course Content

UNIT – I

VLSI Design Methodology: Introduction, Structure Design Strategies: Hierarchy, Regularity, Modularity, and Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design and Platform based design – system on a chip.

Design Flows: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System

Text 1: Chapter 14 **11 Hrs**

Self Learning Components:

Layout Design and Tools: Hierarchical Stick Diagrams, Automatic Layout.

UNIT – II

Design Capture Tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

Text 2: Chapter 17 **10 Hrs**

Self Learning Components:

Design Rules: Scalable Design Rules, Fabrication Errors and Typical Process Parameters.

UNIT – III

Datapath Subsystem Designs: Basic Combinational Components: Decoders, Encoders, Multiplexers, Demultiplexers and Magnitude Comparators.

Basic Sequential Component: Registers, Shift Registers, Counters, and Sequence generators. Shifters, Addition/ Subtraction, Parallel prefix adders, Multiplication: Signed and Unsigned Multipliers and Division.

Memory Subsystems: Introduction: Memory Classification, Memory organization and Memory access timing. Static Random Access Memory (SRAM): RAM Core Structures, Operations of SRAM, Row decoders, Column decoders / Multiplexers, and Sense amplifiers. Dynamic Random Access Memory (DRAM): Cell structures, Structures of Memory array, Read only Memory. Nonvolatile Memory: Flash Memory, other Nonvolatile Memories. Other Memory

Devices: Content Addressable Memory, Register files, Dual port RAM, Programmable logic arrays and FIFO.

Text 2: Chapter 10 and 11 **10 Hrs**

Self Learning Components:

Case study for different types of adder, shifter and multiplier.

UNIT – IV

Power Distribution and Clock Designs: Power Distribution Networks: Design issues of power distribution networks and Power distribution networks. Clock Generation and Distribution Networks: Clock system architectures, Clock Generation circuits and Clock Distribution Networks. Phase-Locked Loops/Delay-Locked Loops: Charge Pump PLLs, All Digital PLLs and Delay Locked Loops.

Input/ Output Modules and ESD Protection Networks: General Chip Organizations: Power Pads and I/O Pads. Input Buffers: Schmitt Circuits, Level-Shifting Circuits and Differential Buffers. Output Drivers / Buffers, Electrostatic Discharge Protection Networks.

Text 2: Chapter 14 and 15 **10 Hrs**

Self Learning Components:

Perform the power analysis for the given digital circuits.

UNIT – V

Design Economics: Nonrecurring Engineering Costs (NREs), Recurring Costs, Fixed Costs, Schedule, Personpower, Project Management, Design reuse.

Testing, Verification, and Testable Designs: An Overview of VLSI Testing: Verification testing, Wafer test and Device test. Fault Models: Stuck at faults, Equivalent faults, Bridge and stuck open / stuck closed faults and delay faults, Fault detection. Automatic Test Pattern Generation, Testable Circuit Designs: Ad hoc Approach, Scan-Path Method and Built-in Self-Test and Boundary-Scan Standard—IEEE 1149.1. System-Level Testing: SRAM BIST and March Test, Core-Based Testing and SoC Testing.

Text 1: Chapter 14 **11 Hrs**

Text 2: Chapter 16

Self Learning Components:

Case Study: VLSI Applications on RISC microcontroller, ATM Switch.

TEXT BOOKS

1. **"Introduction to VLSI Systems : A Logic, Circuit, and System Perspective" ,** Ming-Bo Lin, CRC Press, ISBN-10: 143986859X, ISBN-13: 978-1439868591, 2011
2. **"CMOS VLSI Design: a Circuits and Systems Perspective",** Neil H. E. Weste, David Money Harris, Pearson, 4th edition, ISBN 10: 0-321-54774-8, ISBN 13:978-0-321-54774-3

REFERENCE BOOKS

1. **"Basic VLSI Design**", Douglas A Pucknell and Kamran Eshragian, PHI 3rd Edition, ISBN 13: 9788120309869. (original Edition – 1994).
2. "**Modern VLSI design: System on Silicon" Pearson Education**", Wayne, Wolf, 2nd edition, ISBN: 81-7758-411-1, 1998.

Professional Elective-IV			
Course Title: **RF Integrated Circuits**			
Course Code: **P20MECE253**	Semester: **II**	**L**-T-P-**H** : **4**-0-0-**4**	Credits: **4**
Contact Period : Lecture: **52 Hrs**. Exam: **3 Hrs**.		Weightage: CIE: **50%**	SEE: **50%**

A. Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Apply the knowledge of RF circuits & systems in IC design
2. Analyze CMOS circuits and its impact on Radio frequency IC design.
3. Design and implement RF transceiver chain with specification.
4. Evaluate the different performance parameters used in RF design using CAD tools.

B. Course Content

UNIT – I

Introduction; RF Design Tradeoffs; Fading; Diversity, Multiple Access Techniques; Analog. & Digital. Modulation, S and ABCD parameters; Resonance in LC circuits, Impedance transformations and matching; L-matches Pi- & T-matches; Other matches,- RF Inductors, & Transformers, Capacitors and Varactors . MOS Device Operation,

Text 1: Chapter 3

Text 2: Chapter 3,4,5,7 **11 Hrs**

Self Learning Components:

Read and understand the paper

J.R. Long and M.A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's", IEEE Journal of Solid State Circuits, March 1997.

UNIT – II

Introduction to RF Systems, Basic RF Concepts - Nonlinearity, Time Variance etc IIP3, different expressions/calculations for IIP3, Noise in RF Circuits, Classical Two-port Noise Theory, Noise Figure of Cascaded Systems, Sensitivity, SFDR, MOSFET 2-port Noise Parameters

Text 2: Chapter 11,12

Text 3: Chapter 2 **10 Hrs**

Self Learning Components:

Read and understand the paper

H.T. Friis, "Noise Figures of Radio Receivers," Proceedings of the IRE, July 1944.

UNIT – III

LNA Design; Introduction to Mixers, Two- and Three-port Mixers, Gilbert Mixers
Linearity and Noise of Gilbert Mixers, Other Linearisation Techniques, Other Mixers;

Text 1: Chapter 6

Text 2: Chapter 13

Text 3: Chapter 3 **10 Hrs**

Self Learning Components:

Read and understand the paper

D.K. Shaeffer and T.H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," IEEE Journal of Solid State Circuits, May 1997.

UNIT – IV

Tx Architectures, Rx Architectures: Direct-Conversion Rx, Heterodyne Rx; Image-Reject Rx, VCOs, Colpitts Oscillator; Quadrature Oscillators; Phase Noise - LTI Analysis, Phase Noise - LTV Analysis

Text 1: Chapter 4, 8.

Text 2: Chapter 19 **11 Hrs**

Self Learning Components:

Read and understand the paper

S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," IEEE Communications Magazine, November 2000.

UNIT – V

VCO Wideband Amplifiers Power Amplifiers Analog and RF Layout

Text 1: Chapter 8

Text 3: Chapter 7 **10 Hrs**

Self Learning Components:

Simulate a CMOS Gilbert Mixer using RF Layout principles in Cadence tool.

TEXT BOOKS:

1. **"RF Microelectronics"** Behzad Razavi, 2nd edition, Pearson, ISBN 978-0-13-713473-1.
2. **"The Design Of CMOS Radio-Frequency Integrated Circuits"** Thomas H. Lee, 2nd edition, Cambridge University Press ISBN 0-521-83539-9
3. **"VLSI for Wireless Communication",** Bosco Leung, 2nd edition, Prentice Hall - Electronics and VLSI Series, ISBN 978-1-4614-0985-4.

Laboratory--II			
Course Title: **VLSI and Embedded System Laboratory - II**			
Course Code: **P20MECEL27**	Semester: **II**	L-T-**P-H** : 0-0-**4-4**	Credits:**2**
Contact Period : Lab: **36 Hrs**.; Exam: **3 Hrs**.	Weightage: CIE: **50 %**		SEE: **50%**

A. Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to:

1. Learn DRC, LVS and Parasitic Extraction of the various designs.
2. Design and simulate the various basic CMOS analog circuits and use them in higher circuits like data converters using design abstraction concepts.
3. Understand the specifications and working of Processor.
4. Familiarize display interfacing to the processor.
5. Understand different peripherals interface for multiple real-time experiments.

B. Course Content

A. ANALOG DESIGN

Analog Design Flow:

Design the following circuits with given specifications*, completing the design flow mentioned below:

a. Draw the schematic and verify the following
   DC Analysis, AC Analysis and Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

1. Basic gates and universal gates
2. A Single Stage differential amplifier
3. Common source and Common Drain amplifier
4. Design an op-amp with given specification* using differential amplifier Common source amplifier in library**
5. Design a 4/8 bit R-2R based DAC for the given specification
6. Design a simple 4/8-bit ADC converter using any one of the tools given above

B. Embedded System

1. Interface and Control of on-board LEDs (signaling) through Switch control (Sensors).
2. Interface and smart control of Motors (application specific).
3. Establishing Wired/Wireless Communication using peripherals.
4. Interfacing different Display or Output peripherals with Processor.
5. Measurement of Time and Frequency using Timers and interrupts.
6. Develop a system to count the number of vehicle passed on road. Get the input from relevant sensor and perform the operation.

TEXT BOOKS:

1. **"The Definitive Guide to ARM_ Cortex_-M3 and Cortex-M4 Processors"**, Joseph Yiu, 3rd edition , Newness publications, ISBN 13: 978-0-12-408082-9, 2016**.**
2. **"Design of Analog CMOS Integrated Circuits",** Behzad Razavi, 2nd edition Tata McGraw Hill, ISBN 978-0-07-252493-2 2017.